Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

Claim 1 **(Previously Presented)**: 1. A method of providing a CAM (content addressable memory) cell of a flash memory device, including the steps of:

fabricating a respective core flash memory cell, to be used as the CAM cell, as part of a core array of the flash memory device; and

accessing the respective core flash memory cell as the CAM cell for a CAM function within the flash memory device.

Claim 2 **(Previously Presented)**: The method of claim 1, further including the step of:

fabricating an additional sector as part of the core array of the flash memory device to include the respective core flash memory cell used as the CAM cell.

Claim 3 **(Currently Amended)**: ~~The method of claim 2, further including the step of:~~ A method of providing a CAM (content addressable memory) cell of a flash memory device, including the steps of:

fabricating a respective core flash memory cell, to be used as the CAM cell, as part of a core array of the flash memory device;

accessing the respective core flash memory cell as the CAM cell for a CAM function within the flash memory device;

fabricating an additional sector as part of the core array of the flash memory device to include the respective core flash memory cell used as the CAM cell; and

fabricating within the additional sector a plurality of core flash memory cells, each to be used as a respective CAM cell within the flash memory device.

Claim 4 **(Previously Presented)**: The method of claim 3, further including the step of:

fabricating an additional X-decoder for decoding X-address data during accessing of a

word-line of the additional sector.

Claim 5 **(Previously Presented)**: The method of claim 3, wherein each core flash memory cell within the additional sector corresponds to one of a plurality of other sectors of the flash memory device, and wherein the method further includes the step of:

using sector address bits as Y-address bits that are decoded during accessing of a bit line of the additional sector.

Claim 6 **(Previously Presented)**: The method of claim 5, wherein the sector address bits are decoded with a Y-decoder used for accessing a bit line of the other sectors.

Claim 7 **(Previously Presented)**: The method of claim 3, wherein whether each of the core flash memory cells within the additional sector is programmed or erased indicates whether a corresponding one of a plurality of other sectors is write-protected for write protect (WP) functionality.

Claim 8 **(Previously Presented)**: The method of claim 7, further including the steps of:

generating a control signal to initiate a read on a core flash memory cell within the additional sector before user programming for a selected address within a selected sector of the other sectors;

using a sector address of the selected address to indicate which core flash memory cell within the additional sector is to be read;

reading the programmed or erased state of the core flash memory cell used as a CAM cell corresponding to the selected sector; and

disabling user programming if the core flash memory cell used as the CAM cell corresponding to the selected sector is programmed.

Claim 9 **(Previously Presented)**: The method of claim 8, wherein the step of reading is performed by read/verify circuitry that is also used for reading core flash memory cells of the other sectors.

Claim 10 **(Previously Presented)**: The method of claim 7, further including the steps of:

generating a control signal to initiate a read on a core flash memory cell within the additional sector before user erasing for a selected sector of the other sectors;

using the sector address of the selected sector to indicate which core flash memory cell within the additional sector is to be read;

reading the programmed or erased state of the core flash memory cell used as a CAM cell corresponding to the selected sector; and

disabling user erasing if the core flash memory cell used as the CAM cell corresponding to the selected sector is programmed.

Claim 11 **(Previously Presented)**: The method of claim 10, wherein the step of reading is performed by read/verify circuitry that is also used for reading core flash memory cells of the other sectors.

Claim 12 **(Previously Presented)**: The method of claim 10, wherein the programmed or erased state of each of the core flash memory cells within the additional sector is read to determine which of the other sectors may be erased.

Claim 13 **(Previously Presented)**: The method of claim 7, further including the steps of:

inputting a control signal indicating auto-select mode for reading the programmed or erased state of a selected core flash memory cell within the additional sector; and

reading and outputting the programmed or erased state of the selected core flash memory cell.

Claim 14 **(Previously Presented)**: The method of claim 13, wherein the step of reading is performed by read/verify circuitry that is also used for reading core flash memory cells of the other sectors.

Claim 15 **(Previously Presented)**: The method of claim 7, further including the steps of:

detecting command entry for programming a selected core flash memory cell within the additional sector; and

programming the selected core flash memory cell within the additional sector upon the detection of the command entry for programming the selected core flash memory cell.

Claim 16 **(Previously Presented)**: The method of claim 15, wherein the step of programming is performed by program circuitry that is also used for programming core flash memory cells of the other sectors.

Claim 17 **(Previously Presented)**: The method of claim 7, further including the steps of:

detecting command entry for erasing the additional sector; and

erasing the core flash memory cells within the additional sector upon the detection of the command entry for erasing the additional sector.

Claim 18 **(Previously Presented)**: The method of claim 17, wherein the step of erasing is performed by erase circuitry that is also used for erasing core flash memory cells of the other sectors.

Claim 19 **(Previously Presented)**: A system for providing a CAM (content addressable memory) cell of a flash memory device, comprising:

a respective core flash memory cell fabricated as part of a core array of the flash memory device and to be used as the CAM cell;

a Y-decoder for accessing a bit line of the core array of the flash memory device including a bit line of the respective core flash memory cell used as the CAM cell; and

an X-decoder for accessing a word-line of the respective core flash memory cell used as the CAM cell for a CAM function within the flash memory device.

Claim 20 **(Currently Amended)**: ~~The system of claim 19, further comprising:~~ A system for providing a CAM (content addressable memory) cell of a flash memory device, comprising:

a respective core flash memory cell fabricated as part of a core array of the flash memory device and to be used as the CAM cell;

a Y-decoder for accessing a bit line of the core array of the flash memory device including a bit line of the respective core flash memory cell used as the CAM cell;

an X-decoder for accessing a word-line of the respective core flash memory cell used as the CAM cell for a CAM function within the flash memory device;

an additional sector fabricated as part of the core array of the flash memory device to include the respective core flash memory cell used as the CAM cell; and

an additional X-decoder unit for accessing a word-line of the additional sector.

Claim 21 **(Previously Presented)**: The system of claim 20, wherein the additional sector includes a plurality of core flash memory cells, each to be used as a respective CAM cell within the flash memory device.

Claim 22 **(Previously Presented)**: The system of claim 21, wherein each core flash memory cell within the additional sector corresponds to one of a plurality of other sectors of the flash memory device.

Claim 23 **(Previously Presented)**: The system of claim 22, wherein the Y-decoder decodes sector address bits as Y-address bits during access of a bit line of the additional sector.

Claim 24 **(Previously Presented)**: The system of claim 22, wherein whether each of the core flash memory cells within the additional sector is programmed or erased indicates whether a corresponding one of the other sectors is write-protected for write protect (WP) functionality.

Claim 25 **(Previously Presented)**: The system of claim 24, further comprising:

write protect operation logic for detecting entry into one of write protect read, write

protect program, and write protect erase operations.

Claim 26 **(Previously Presented)**: The system of claim 25,

wherein the write protect operation logic generates a control signal to initiate a read on a core flash memory cell within the additional sector before user programming for a selected address within a selected sector of the other sectors;

and wherein the Y-decoder uses the sector address of the selected address to indicate which core flash memory cell within the additional sector is to be read;

the system further comprising:

read/verify circuitry and a latch for reading the programmed or erased state of the core flash memory cell used as a CAM cell corresponding to the selected sector; and

a back-end state machine for disabling user programming if the core flash memory cell used as the CAM cell corresponding to the selected sector is programmed.

Claim 27 **(Previously Presented)**: The system of claim 26, wherein the read/verify circuitry is also used for reading core flash memory cells of the other sectors.

Claim 28 **(Previously Presented)**: The system of claim 25:

wherein the write protect operation logic generates a control signal to initiate a read on a core flash memory cell within the additional sector before user erasing for a selected sector of the other sectors;

and wherein the Y-decoder uses the sector address of the selected sector to indicate which respective core flash memory cell within the additional sector is to be read;

the system further comprising:

read/verify circuitry and a latch for reading the programmed or erased state of the core flash memory cell used as a CAM cell corresponding to the selected sector; and

a back-end state machine for disabling user erasing if the core flash memory cell used as the CAM cell corresponding to the selected sector is programmed.

Claim 29 **(Previously Presented)**: The system of claim 28, wherein the read/verify

circuitry is also used for reading core flash memory cells of the other sectors.

Claim 30 **(Previously Presented)**: The system of claim 25,

wherein the write protect operation logic inputs a control signal indicating auto-select mode for reading the programmed or erased state of a selected core flash memory cell within the additional sector;

the system further comprising:

read/verify circuitry and a latch for reading and outputting the programmed or erased state of the selected core flash memory cell.

Claim 31 **(Previously Presented)**: The system of claim 30, wherein the read/verify circuitry is also used for reading core flash memory cells of the other sectors.

Claim 32 **(Previously Presented)**: The system of claim 25,

wherein the write protect operation logic detects command entry for programming a selected core flash memory cell within the additional sector;

the system further comprising:

program circuitry for programming the selected core flash memory cell upon the detection of the command entry for programming the selected core flash memory cell.

Claim 33 **(Previously Presented)**: The system of claim 32, wherein the program circuitry is also used for programming core flash memory cells of the other sectors.

Claim 34 **(Previously Presented)**: The system of claim 25,

wherein the write protect operation logic detects command entry for erasing the additional sector;

the system further comprising:

erase circuitry for erasing the core flash memory cells within the additional sector upon the detection of the command entry for erasing the additional sector.

Claim 35 **(Previously Presented)**: The system of claim 34, wherein the erase circuitry is also used for erasing core flash memory cells of the other sectors.